Low Power and High Speed Architecture for 32-Bit ALU Design

Sreenivasa Rao.Ijjada, D.Srinivas and Dr.V.Malleswara Rao

Abstract – Low power and high speed is challenging work in processor design. Implementing power optimization on all components of the processor is a choise.One of the most basic component in the processor is the ALU. The Arithmetic and Logic Unit (ALU) is a combination circuit that performs a number of arithmetic and logical operations within a processor. The most research on the power consumption of circuits has been concentrated on the switching power and the power dissipated by the leakage current has been relatively minor area. In today's IC design, one of the key challenges is the increase in power dissipation of the circuit which in turn shortens the service time of battery-powered electronics, reduces the long-term reliability of circuits due to temperature-induced accelerated device and interconnects aging processes, and increases the cooling and packaging costs of these circuits. In this paper the main aim is to reduce power dissipation. The architecture of ALU has several implications on power consumption, delay and area. This paper proposes a new design method for 32-bit ALU design, which is low power and high speed compared to general CMOS 32 bit ALU logic. It is based on controlling leakage currents through Leakage Controlled Transistor and calculated the power dissipation, uses TANNER EDA Tools for schematic layout simulation as well as the schematic versus layout comparison. The simulation technology used is MOSIS 250nm.

KEYWORDS –ALU, Low power, LCT, STACK EFFECT

1 INTRODUCTION

An ALU combines a variety of arithmetic and logic operations into a single unit. For examples, addition, subtraction, AND, NAND, OR, NOR, XOR and XNOR. The bitwise output results in the 8X1 multiplexer .Each of the single bit building blocks are cascaded together to form a 32 bit ALU. Since the architecture of ALU has several implications on power consumption, delay, and area, then how to organize the operations is a problem. The top-level module consists of a 32 bit ALU..Power dissipation is a major concern in the VLSI circuit design for CMOS technology. CMOS technology has been scaled down from 1um to 32nm over last decade. Technology scaling reduces gate oxide thickness and gate length which increases transistor density and reduces the circuit delay. Scaling down gate lengths increase leakage power dissipation due to the reduced

(Sleep transistor) in the path between the supply voltage and ground. The sleep transistor is turned on when the circuit is active and turned off when the circuit is in the idle state with the help of sleep signal. This creates virtual power and ground rails in the circuit. Hence, there is a significant detrimental effect on the switching speed when the circuit is active. The identification of the idle regions of the circuit and the generation of the sleep signal need additional hardware capable of predicting the circuit states accurately.

This additional hardware con sumes power throughout the circuit operation even when the circuit is in an idle state to continuously monitor the circuit state and control the sleep transistors. The use of multiple threshold voltage CMOS (MTCMOS) technology for leakage control is described in [3] and [4]. The transistors of the gates are at low threshold voltage and the ground is connected to the gate through a high-threshold voltage NMOS gating transistor. The logical function of a gating transistor is similar to that of a sleep transistor. A variation of MTCMOS technique is the Dual technique, which uses transistors with two different threshold voltages. Low-threshold transistors are used for the gates on the critical path and high-threshold transistors are used for those not in the critical path [8], [5], [6]. These techniques are not effective in controlling the leakage power when the circuit is in active state. In [7], the authors use the concept of forced stacks for leakage control. Forced stacking introduces an additional transistor for every input of the gate in both N and P networks. This ensures that two transistors are OFF instead of one for every OFF-input of the gate and hence makes a significant savings on the leakage current. However, the loading requirements for each input introduced by the forced stacking reduce the drive current of the gate significantly. This results in a detrimental impact on the speed of the circuit. In [2], a blend of sleep transistors and the stacking effects are used to reduce leakage power. This method identifies a circuit input vector for which the leakage current of the circuit is the lowest possible.

- *Sreenivasa Rao.Ijjada, Asst.Professor, ECE dept, GIT, GITAM University, Visakhapatnam, AP, INDIA*
- *D.Srinivas M.tech student, VLSI, GIT, GITAM University*
- *Dr.V.Malleswara Rao, Prof & HOD, ECE dept, GIT, GITAM Universi-*

The sleep signal controlled transistors are inserted away from the critical path where only one transistor is OFF when low-leakage input vector is applied to the circuit. Hence, this technique is input-vector dependent. Moreover, as this technique uses sleep transistors, it needs additional hardware for controlling them.This additional hardware consumes power in both idle and active states of the circuit

In this work, we develop a new technique for leakage control in CMOS circuits. The proposed technique avoids the problems associated with the technique discussed above.

2 CMOS LOGIC ALU DESIGN

2.1 1BIT ALU

The block diagram of basic one bit ALU is shown in the **Fig.1**. CMOS Design methodology consists of eleven components.

a. INVERTER: The inverter consists of an NMOS and a PMOS connected in series. The PSWITCH is connected from a '1' source i.e. the VDD to the output and input The NSWITCH is connected from a '0' source i.e. the GND to the output and the input.

b. NAND GATE: The CMOS NAND gate is derived examining the K-MAP. The '0' dictates the AND structure which is constructed using two NMOS in PARALELL. The '1' dictates the OR structure which is constructed using two P-MOS connected in SERIES.

c. AND GATE: The CMOS AND gate has been designed by inverting the CMOS NAND gate. The output of AND is high only when both the inputs are high i.e. the output is low when any one of the inputs is low.

d. NOR GATE: The CMOS NOR gate is derived examining the K-MAP. The '0' dictates the AND structure which is constructed using two NMOS in parallel. The '1' dictates the OR structure which is constructed using two P-MOS connected in series.

e. OR GATE: The CMOS OR gate has been designed by inverting the CMOS NOR gate. The output of OR is high only when both or any one of the inputs is high i.e. the output is low only when both the inputs are low.

f. XOR GATE: The Exclusive-OR, or XOR function can be described verbally as, "Either A or B, but not both." The output of an XOR gate is high only when any one of the inputs is low i.e. for the output of the XOR gate to be high both the inputs should be either high or low. A XOR gate can be designed by a combination of NAND and OR gates.

g. XNOR GATE: The XNOR gate is designed by inverting the XOR gate .The output of the XNOR gate is high when both the inputs are low and both the inputs are high. A CMOS representation of the XNOR

h. FULL-ADDER: The full-adder circuit adds three one-bit binary numbers (C A B) and outputs two one-bit binary numbers, a sum (S) and a carry (C). The full-adder is usually a component in a cascade of adders, which add 8, 16, 32, etc. binary numbers. The output of XOR gate is called SUM, while the output of the AND gate is the CARRY.The AND gate produces a high output only when both inputs are high. The XOR gate produces a high output if either input, but not both, is high. The 'C' for an ADDER is always made low

i. SUBTRACTOR: Binary subtraction is performed by adding the two's compliment of the number to be subtracted. 2's compliment of a number can be achieved by inverting the number and adding one to it. This is achieved by inverting each bit of the number to be subtracted and adding '1' by means of the carry-in. The carry-in of a Subtractor must be '1'.

j. MULTIPLXER: A multiplexer is a combinatorial circuit that is given a certain number (usually a power of two) data inputs, let us say 2n, and n address inputs used as a binary number to select one of the data inputs. The multiplexer has a single output, which has the same value as the selected data input. In the present design an 8x1 Multiplexer has been used for each single bit out depending on input needed to send out. This also ensures a faster ALU as the functions are performed as soon as the input is fed to the ALU. The 3 control signals (S [2-0]) show the desired output in the order as shown below:

000→ADDITION
001→AND
010→NAND
011→ OR
100→NOR
101→XOR
110→XNOR
111→SUBTRACTION

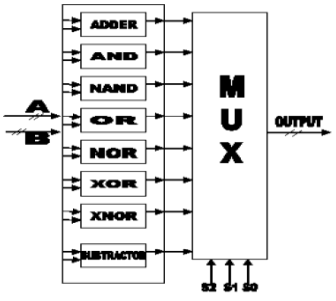


Fig 1. Block diagram of Basic 1-BIT ALU

The Schematic diagram of 1 bit ALU with CMOS logic is shown in **Fig.2**, all the eight operations such as addition, subtraction, AND, NAND, OR, NOR, XOR, XNOR operation s and a eight input multiplexer are designed using CMOS logic

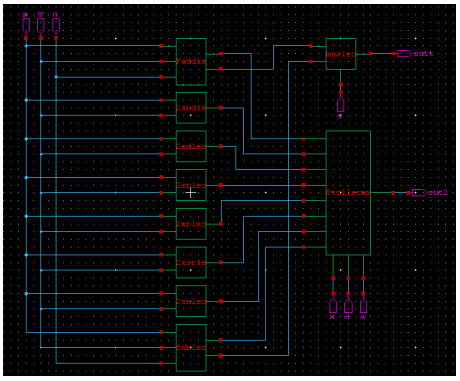


Fig 2. SCHEMATIC FOR 1-BIT ALU

2.2 32 BIT ALU

Depending upon the multiplexer select inputs the eight operations can be verify, here 32 bit sequence is taken as an input and randomly verify the output for the 32 bit full adder operation. In this paper each of the single bit ALU are cascaded to form a 32 bit ALU. The top-level module consists of a 32 bit ALU shown in **Fig.3**

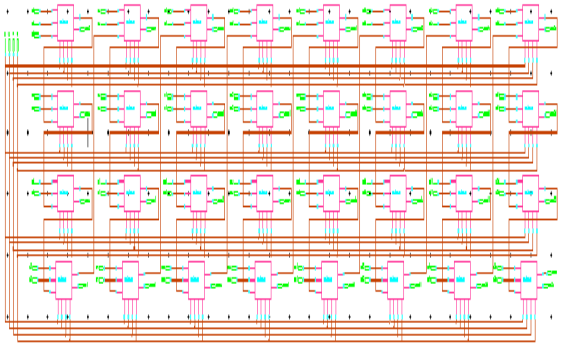


Fig 3. SCHEMATIC OF CMOS 32-BIT ALU

3. PROPOSED DESIGN TECHNIQUE

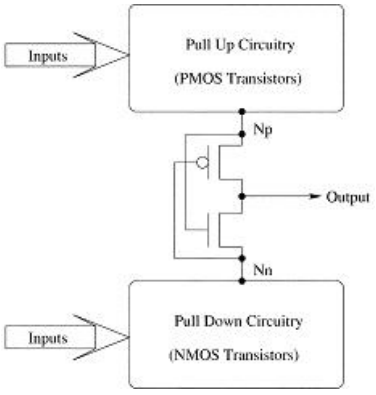


Fig 4. Generalized structure for leakage control gates

Two leakage control transistors (a p-type and a n-type) shown in **Fig.4** are introduced within the logic gate for which the gate terminal of each leakage control transistor (LCT) is controlled by the source of the other.

In this arrangement, one of the LCTs is always "near its cutoff voltage" for any input combination. This increases the resistance of the path from Vdd to ground, leading to significant decrease in leakage currents. The gate-level net list of the given circuit is first converted into a static CMOS complex gate implementation and then LCTs are introduced to obtain a leakage-controlled circuit. The significant feature of LECTOR is that it works effectively in both active and idle states of the circuit, resulting in better leakage reduction.

The basic idea behind the approach for reduction of leakage power is the effective stacking of transistors in the path from supply voltage to ground.

3.1 32 BIT ALU WITH PROPOSED TECHNIQUE

In this paper each of the single bit ALU are cascaded to form a 32 bit ALU. The Schematic of 32 bit ALU with the proposed leakage controlled technique is shown in the **Fig.4**. An eight function instruction set ALU performs the following: addition, subtraction, AND, NAND, OR, NOR, XOR and XNOR.The bitwise output results in the 8X1 multiplexer. Each of the single bit building blocks shown in **Fig.5** are cascaded together to form a 32 bit ALU.

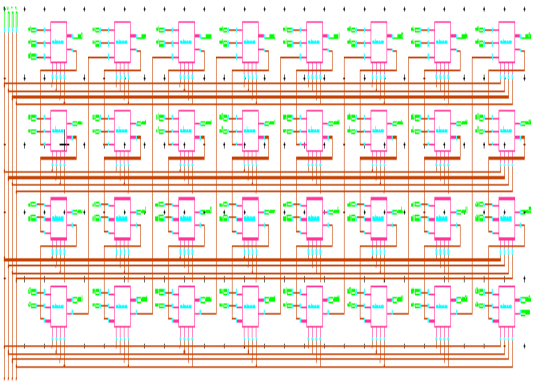
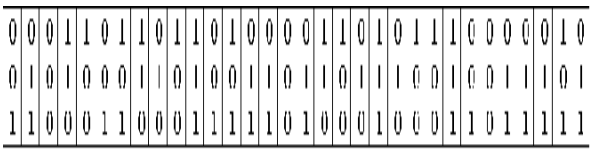


Fig 4.SCHEMATIC OF 32-BIT ALU WITH PROPOSED TECHNIQUE

4. RESULTING OUTPUT WAVE FORMS

When the 32 bit random input sequence is considered, When cin=1, a0 to a31, b0 to b31 the output of full adder is shown in Table 1

TABLE 1: 32 BIT INPUT AND OUTPUT SEQUENCE



Output waveforms for the above in the CMOS logic 32 bit ALU are shown in **Fig.7**

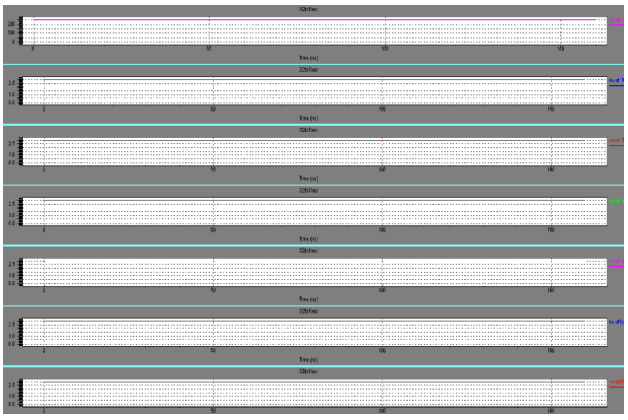


Fig .7 OUTPUT WAVEFORMS FOR 32-BIT ALU USING CMOS LOGIC

Output waveforms of 32 bit ALU with Proposed logic are shown and **Fig.8**

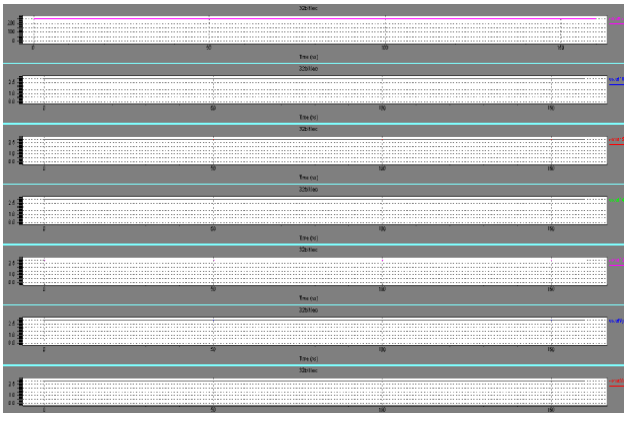


Fig8. OUTPUT WAVEFORMS FOR 32-BIT ALU USING LECTOR TECHNIQUE

5. OBSERVATIONS

TABLE 2: POWER DISSIPATION FOR FULLADDER AT 4°C TEMPERATURE

S. No	Technique	Power Dissipation
1	CMOS	0.0677085µw
2	LECTOR	0.0508083 µw

TABLE 3: POWER DISSIPATION FOR FULL ADDER AT 25°C TEMPERATURE

S. No	Technique	Power Dissipation
1	CMOS	0.09821352 µw
2	LECTOR	0.0736635 µw

TABLE 4: POWER DISSIPATION FOR FULL ADDER AT 60OC TEMPERATURE

S. No	Technique	Power Dissipation
1	CMOS	0.18340506 µw
2	LECTOR	0.14841623 µw

6. CONCLUSION

In this paper 250nm technology has been adopted and the 32 bit ALU circuit is implemented using TANNER tools. Nearly 25% reduction has been observed in the power dissipation after the implementation of the LECTOR technique.

7. REFERENCES

[1] M. D. Powell, S.-H. Yang, B. Falsafi, K. Roy, and T. N. Vijaykumar, "Gated-Vdd: A circuit technique to reduce leakage in deep submicron cache memories," in *Proc. IEEE ISLPED*, 2000, pp. 90–95.

[2] M. C. Johnson, D. Somasekhar, L. Y. Chiou, and K. Roy, "Leakage control with efficient use of transistor stacks in single threshold CMOS,"
IEEE Trans. VLSI Syst., vol. 10, pp. 1–5, Feb. 2002.

[3] J. Kao, A. Chandrakasan, and D. Antoniadis, "Transistor sizing issues and tool for multi-threshold CMOS technology," in *Proc. 34th DAC*, 1997, pp. 409–414.

[4] C. Gopalakrishnan and S. Katkoori, "Resource allocation and binding approach for low leakage power," in *Proc. IEEE Int. Conf. VLSI Design*,Jan. 2003, pp. 297–302.

[5] L. Wei, Z. Chen, M. Johnson, and K. Roy, "Design and optimization of low voltage high performance dual threshold CMOS circuits," in *Proc.35th DAC*, 98 489–492.

[6] V. Sundarajan and K. K. Parhi, "Low power synthesis of dual threshold voltage CMOS VLSI circuits," Proc. IEEE ISLPED, pp. 139–144, 1999.

[7] S. Narendra, S. Borkar, V. De, D. Antoniadis, and A. P. Chandrakasan, "Scaling of stack effect and its application for leakage reduction," Proc. IEEE ISLPLED, pp. 195–200, Aug. 2001.

[8] Q. Wang and S. Vrudhula, "Static power optimization of deep sub-micron CMOS circuits for dual V technology," in Proc. ICCAD, Apr. 1998, pp. 490–496.

[9] S. Sirichotiyakul, T. Edwards, C. Oh, R. Panda, and D. Blaauw, "Duet: An accurate leakage estimation and optimization tool for dual-V circuits,"
IEEE Trans. VLSI Syst., vol. 10, pp. 79–90, Apr. 2002.

[10] Kim Se Hun and V.J Mooney, "Sleepy Keeper: A New Approach to Low-leakage Power VLSI Design", *IFIP International Conference on Very Large Scale Integration*, pp. 367-372, Oct., 2006.

8. AUTHORS

1) Mr.I.Sreeenivasa Rao received his AMIE degree from The Institution of Engineers (INDIA), Kolkata in the year 2001 and He received his M.Tech degree in the year 2006 from J.N.T.U. Kakinada. He is a Ph.D Scholar and working in GITAM Institute of Technology, GITAM University, and Visakhapatnam as an Assistant Professor. He is a life member of AMIE. His research activities are related to Low Power VLSI Design.

2) Dr.V.Malleswara Rao received his B.E degree from Andhra University in the year 1985 and received M.E degree in the year 1989 from Andhra University and completed his Ph.D from J.N.T.U Hyderabad and working in GITAM Institute of Technology, GITAM University, Visakhapatnam as Professor and H.O.D. He is a life member of AMIE. His research activities are related to Low Power VLSI Design, Microwave&Signal Processing.