Fusion of VLSI & Signal processing Technologies for the Enhancement in Wireless Communications

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Abstract: Wireless communication system is a heavy dense composition of signal processing techniques with semiconductor technologies. With the ever increasing system capacity and data rate, VLSI design and implementation method for wireless communications becomes more challenging, which urges researchers in signal processing to provide new architectures and efficient algorithms to meet low power and high performance requirements. This paper presents a survey of recent research, a development in VLSI architecture and signal processing algorithms with emphasis on wireless communication systems. It is shown that while contemporary signal processing can be directly applied to the communication hardware design including ASIC, SoC, and FPGA, much work remains to realize its full potential. It is concluded that an integrated combination of VLSI and signal processing technologies will provide more complete solutions.

I. INTRODUCTION

Since the concept of wireless mobile systems was invented at the Bell Laboratories in the mid of twentieth century, it has been revolutionized into a multibillion dollar industry that changes the way people communicate with each other everyday. As Cloude Shannon incepted the fundamental mathematical theory of communication, modern wireless communication technology has also been developed extensively in both information theory and digital communication areas. It has gone through an evolution of three generations including AMPS, PCS/TDMA and CDMA/UMTS technologies. There is no doubt that wireless mobile communication is still one of the most dominant rapid-growing businesses in the near future. When high-speed data service becomes widely available and affordable to mobile subscribers, the wireless technology could edge the long-stand competition against the wire line systems. In the author's point of view, there are probably two major driven forces behind the ever improving wireless systems, VLSI technology and advanced digital signal processing.

Semiconductor technology is the physical supporter behind wireless communication and signal processing. Complementary MOS technology (CMOS) has been dominant in dynamic digital logic since the late 80's. It has the advantages of low power and high noise margin that are two key characteristics for dynamic digital devices. Accompany with the advancement of high-density wafer fabrication and verification technologies, VLSI actually turns the complicated communication systems into reality. At the early stage of radio communication, the terminals were in the size of a brief-case, while the state-of-the-art mobile device can be clipped in the pocket. On the analog side, Gallium Arsenide (GaAs) design is a major technology breakthrough in recent years that eliminates the old-fashion "tuning radio" systems. A high performance GaAs IC can operate at several Giga Hertz while drawing only a minimal amount of power from a low-voltage supply. This results in a more compact design for base stations and mobile terminals. As the development and manufacturing yields improve further, GaAs will dominate the radio frequency (RF) device market. On the digital side, CMOS wireless transceiver becomes available because of the rapid progress in semiconductor and the digital IC technologies. As the analog-to-digital (A/D) and D/A moving closely to the amplifier and antenna side, it facilitates the digital implementation of transceiver. Meanwhile, the application-specific integrated circuit (ASIC), fueled by the VLSI technology, is developed to accommodate both requirements in clock speed and gate capacity.

Recent announcement by IBM shows that ASIC design is approaching GHz clock-speed and hundred-million gates capacity. It can be predicted that heavy-dense single-chip digital transceivers will be the next attractive competitions among the major wireless infrastructure suppliers. With the ever increasing gate size and computational capacity, ASIC technology evolutes into system-on-a-chip (SoC), a technology trend that would eventually change the methodology of traditional hardware design.

The organization of this paper is as follows. In section 3 a brief background review of VLSI signal processing and its recent development is presented. From a standing point of wireless communication, Section 4 discusses the contemporary issues and challenges of VLSI signal processing for hardware design. Section 5 facilitates case studies to provide examples of efficient design and implementations of pipelined and recursive structures. We conclude in Section 6 with some predictions about the future of VLSI signal processing research in wireless communication.

II. DSP AND VLSI INTEGRATION

General digital signal processing (DSP) processor becomes widely used these days in almost every market of consumer electronics, computers, communications and networking systems. Retrospectively, it is found that DSP system was also driven by VLSI design and semiconductor technology. Since the first DSP processor introduced by Texas Instrument in 1988, its spectacular expansion in the applications is facilitated by the exponential growth complexity offered by the integrated circuit technology, commonly known as Moore's law [2]. As the semiconductor evolutes from micrometer (μm) to nanometer (nm) technologies, the DSP processor clock rate has been elevated from a few to hundreds of megahertz (MHz). While general DSP still remains popular in many areas today, signal processing is reaching to a point far beyond that general DSP processor can handle in terms of capacity and performance requirement, especially in the communication and networking area. ASIC or application-specific signal processor (ASSP) can be uniquely designed to implement the complex signal processing algorithms using highly pipelined multiprocessing architectures. With less consideration of general programmability, the speed performance and power consumption of ASIC or ASSP are much better than general DSP processor. While signal processing research supplies the algorithms to further improve the quality and capacity of wireless communication systems, VLSI design and implementations play a crucial role in turning theory into reality. Therefore, both signal processing and VLSI technologies should be iteratively developed in a parallel form.

III VLSI AND SIGNAL PROCESSING OVERVIEW

. The research in the area of VLSI signal processing has enjoyed a surge of interests during the last decade. The signal processing revolution is largely driven by the flourish semiconductor industry and communication technologies. Historically, modern signal processing algorithms defined a heterogeneous architecture platforms, including microprocessors, digital signal processor (DSP), application-specific integrated circuit (ASIC), and system on a chip (SoC). Communication system is a heavy dense composition of signal processing algorithm and information theories. With the ever increasing system capacity and data rate, VLSI design and implementation method for telecommunication systems becomes more challenging, which urges researchers in signal processing area to provide new architectures and efficient algorithms to meet heavy computation and high performance requirements. Therefore, research in VLSI signal processing is critical in the advancement of telecommunications and integrated circuit technologies.

Because of its widespread practice in advanced computer and communication technologies, DSP algorithms themselves are being subjected to more demanding innovations. As information-age industries constantly reinvent ASIC chips to pursue high-performance lower-power design, there is a constant need for research collaborations in VLSI signal processing. The research in this subject is to design and develop new architectures, algorithms and techniques for VLSI implementation of signal processing.

During the last decades, institutional researchers and industrial engineers have made significant progress in the VLSI signal processing area. One of the most important contributions was the study of signal processing algorithms for high-speed low-power VLSI design. Many algorithms, such as Cordic algorithm, systolic array, bit-series, digit-series and et al, have been well studied and analyzed to accomplish high-speed low-power design for signal flow architecture . Low-power CMOS design was one of the major issues for algorithm-based design and implementations. Systolic array design methodology was well studied using mapping techniques. In this subsection, algorithm-based low-power high-performance multimedia signal processing was the main developing topic. Real-time application drives the algorithm designer to meet both the speed and performance requirements. Pipeline and parallel structure are commonly used to improve the throughput of signal processing data flows. Given the limitation of system clock rate, a general signal processing algorithm may be modified to meet the speed requirement with little scarification in performance. This field of study bridges the gap between algorithm designer and circuit designer.

Another important aspect of VLSI signal processing research is to investigate the fundamental building blocks (or library cells) for telecommunication system, commonly referred as intellectual properties (IP). Shrinking circuit feathers and rising transition density have spawned the astonishing large system-on-a-chip (SoC). Transistor deployment and simulation has surpassed the capacity of an ASIC design team. Modern SoC design method has to surpass the register transport level (RTL) design process. To build a system on a chip, a design house or semiconductor company will have to use a set of multiple IP cores acquired from out-sourced IP providers. Many research institutions and companies have contributed extensively on the IP development for wireless communications, including digital radio transceiver, voice over IP (VoIP) protocol, intelligent antenna (IA), Viterbi decoder, turbo decoder, digital IF channel filter, Bluetooth chipset and many others. These IP cores are usually designed, synthesized and laid out with VLSI tools, and become marketable stand-alone packages. Those ready-to-use IP cores are well positioned in the frontier of the communication industry. The research works in this direction are likely to continue and grow along with the presence of new signal processing algorithms.

The successful story of general-purpose DSP in the last decade is well known in the industry. However, VLSI

signal processing implementations are far beyond the concept and structure of general purpose DSP processors.

In telecommunication networks, a simple system usually consists of many signal processing devices varying in size and capacity. These devices include ASIC, FPGA, ASSP, DSP, PLD and et al. A general DSP processor normally has the advantage of software controlled programmability, but it generally has very limited computational resources with only a single or dual built-in processing threads. Complicated signal processing algorithms for telecommunication require high-performance large-capacity device to accommodate the implementations. Therefore, hundreds of millions of ASIC chip sets are designed and manufactured to carry the processing task in commercial telecommunication systems. These arguments demonstrate that VLSI design method and semiconductor technologies are mainly driven by the high-density integration of signal processing implementations. In contrast, VLSI chip design provides a hardware platform to apply the advanced signal process algorithms to real-time systems.

As semiconductor industries move towards nanotechnologies, it will create ampere space for researchers in signal processing to implement extremely complicated algorithms. In prospective, VLSI signal processing remains as one of key technical areas that requires both the knowledge of VLSI and digital signal processing to design more affective and more efficient telecommunication systems.

IV CONTEMPORARY ISSUES IN WIRELESS & COMMUNICATION HARDWARE DESIGN

Most of the signal processing or communication algorithms are not initially targeted for VLSI implementations. In recent years, researchers in wireless communication area have developed a considerably large amount of advanced algorithms through modeling and simulation. These algorithms are generally proposed and initialized with significant performance improvement. Unfortunately, it is not unusual to learn from the field engineers that the actual implementation of the algorithm on given hardware platform hardly reaches the same level of performance as indicated in computer simulations. There are several possible reasons that could contribute to the discrepancies between design and simulation. The algorithm simulation, generally performed using high-level languages with floating-point operations, has potential issues while matching with a fixed-point hardware design. For a large system such as the entire physical layer of mobile communication, it is difficult to simulate the entire system to the level of details for each bit or symbol. From VLSI design point of view, there are also challenges to model and simulate a multi-million gates ASIC or SoC to process a relatively large set of data samples. This section presents the contemporary issues and challenges for VLSI signal processing in wireless communication.

4.1 BIT-EXACT DESIGN MODELING

The hardware design process is to translate the sophisticated signal processing algorithm into fixed-point hardware gates or standard library cells. Generally a high-level signal processing algorithm designer does not always consider the effects of fixed-point quantization issues. Even though a design of floating-point arithmetic logic unit has been available for a long time, a complete design of signal processing flow in floating-point does not yet exist largely due to its design complexities and hardware costs. Bit-exact modeling of a sophisticated signal processing algorithm to match hardware design is still a remaining issue in VLSI signal processing research.

An emerging technique, called C-model, is getting attraction from both algorithm and circuit designers. It keeps the property of using high-level language for simulation and modeling that favors the traditional algorithm designer. It also includes the concept of dynamic range. In practice, it employs integer operations with consideration of truncation and saturation effects. The concept of C-model is designated to bridge between the algorithm simulation and hardware modeling. Preliminary experiments shows that C-model simulation is about 2~5 magnitudes faster than hardware description language (HDL) model simulation. The goal of C-model development is to achieve bit-exact matching with the actual hardware design. The formal method of this technique is still not yet defined. The semantics and grammar extension for C-model design requires contributions and acceptance from both VLSI and signal processing parties. Therefore, it is expected that bit-exact modeling techniques will attract more attentions in VLSI signal processing research community.

4.2 HETEROGENEOUS ARCHITECTURE FOR SIGNAL PROCESSING

As we pointed out in the Section 3, pipeline techniques and parallel structures have been well studied for implementation of signal flows. In literature, it reveals many techniques to implement signal flow algorithms, such as filters, with a minimal number of logic gates to produce high throughput. However, many DSP algorithms are much more complicated than filters and flow processing. It involves recursive, iterative or adaptive algorithms in order to solve complicated signal processing problems. Adaptive coding in wireless communication is one example. Traditionally, iterative loops can be processed conveniently by a type of instruction-set processor. A heterogeneous architecture should include high-throughput parallel processing units as well as serial processing units for recursive or iterative operations. To the author's knowledge, there is no existing design method available for this type of heterogeneous architecture.

It is not a completely new idea to incorporate an embedded processor (core) into a signal processing ASIC. However, an embedded processor, such as a Power PC core, requires a large number of logic gates and recourses. If a given signal processing algorithm involves mainly a structure-type processing, it is not worth to include an embedded processor into the design. Furthermore, it is not feasible to include for ASIC devices relatively small in size. Now, it urges novel architectures and designs to accommodate the requirement of heterogeneous processing units. A custom-type serial processor design with less logic gates will prevail in the heterogeneous VLSI signal processing architecture.

4.3 VLSI SIGNAL PROCESSING EMULATION

Upon completion of signal processing algorithm design and simulation, VLSI designers undertake the job to implement it with ASIC design representations. It is well known that wafer fabrication is an expensive process in silicon device manufacturing. Therefore, VLSI design verification becomes necessary before release it to the foundry. The state-of-the-art software simulator is able to load a multi-million gates ASIC design synthesis on a powerful workstation providing enough memory space. But the actual simulation time makes it impractical for design verification. Experiment shows that a standard design with 8 million-gates takes about 24 hours to run through 1000 samples of data on a 2 GHz workstation. In practice, it may require a complete set of tests with many different configurations or scenarios. The emulation techniques for VLSI signal processing are expected to replace the time-consuming software simulation.

Signal processing algorithm designers use the emulation platform to demonstrate real-time performance for functional verification. Many practical ASIC implementation issues can be encountered and resolved at the emulation stage. This would significantly shorten the design cycles between algorithm simulations and hardware representations. As the clock speed and gate size of ASIC device increases, it is a challenge for engineers to establish a corresponding emulation system. In recent years, FPGA device has enjoyed a surged expansion both in capacity and speed grid.

A state-of-the-art FPGA device contains more than 6 million logic gates, and it can operate at more than 800 MHz. This makes a high-speed large-scale emulation platform physically possible. However, there remain many practical issues to convert an ASIC design into a FPGA-based emulation platform. It is almost evitable to modify the ASIC synthesis body before emulations due to the architectural difference between ASIC and FPGA. The memory hierarchies and instantiations are also quite different from each other. In fact, the clock speed of FPGA devices may never catch up with ASICs due to its intrinsic complexity, and retiming technique is necessary to emulate the design in sub-clock speed domain. Emulation techniques for VLSI signal processing play an important role in accelerating design verifications.

V CASE STUDY

In this section, we present two design cases to illustrate the studies of VLSI signal processing. Decimation filter design using pipelined structure is described with diagrams. For recursive algorithms, such as a IIR filter, sampling rate issues at the hardware implementation stage are discussed.

CASE STUDY (I): PIPELINED POLYPHASE FIR FILTER

A low-pass filter is designed to decimate the sampling data rate from 92.16 MHz to 30.72 MHz. These frequency ranges are commonly used in CDMA radio transceivers. As listed in Table 1 for Texas Instrument GS-40 0.13 μm technology, multipliers cost more logic gates than adders and registers. Also, to construct the same type of element, it needs more gates for higher speed operation. This is largely due to the internal pipelines used by high-speed multiplier or adder.

As shown in Figure 1, the in-phase (I) and in-quadrate (Q) data samples are pipelined before entering to the filter structure. Taking advantage of Polyphase architecture, three sections of sub-filters are time-multiplexed to share the same multiplier. This cuts the total number of multipliers from 54 down to 9, and it reduced the total gate count considerably. It is worth to note that quantization effect has been considered for the pipelined FIR design. Simulation has been performed to obtain the optimal bit-width at each stage, including multipliers, adder trees and the final summations. Insufficient bit-width resolution would degrade the performance of signal processing noticeably.

Error vector magnitude (EVM) is a common measurement on performance degradations in communication systems. Lower EVM number is desirable. But it generally results in more bit-width of the signals, and it effectively prompts for more logic gates in hardware. Therefore, both input and output signals should be characterized properly to obtain the best trade off between the EVM number and actual gate-size.

CASE STUDY (II): DOUBLE SAMPLING RATE RECURSIVE IIR

Implementation of IIR filter is different from FIR because of its recursive property. Simple first-order IIR filters are widely used in communication systems. It can be used as a tracking factor in the automatic gain control (AGC) system block. The system function is stated as,

$$H(z) = \frac{a}{1-(1-a)z^{-1}} \qquad (1)$$

Circuit Element	1-bit Register	16x16 Multiplier (100 MHz)	16x16 Multiplier (200 MHz)	16-bit Adder (100 MHz)	16-bit Adder (200 MHz)	Multiplexer
Number of Gates	10	4526	18759	682	351	2

Table 1. Approximate number of gates for each circuit element (TI-GS40)

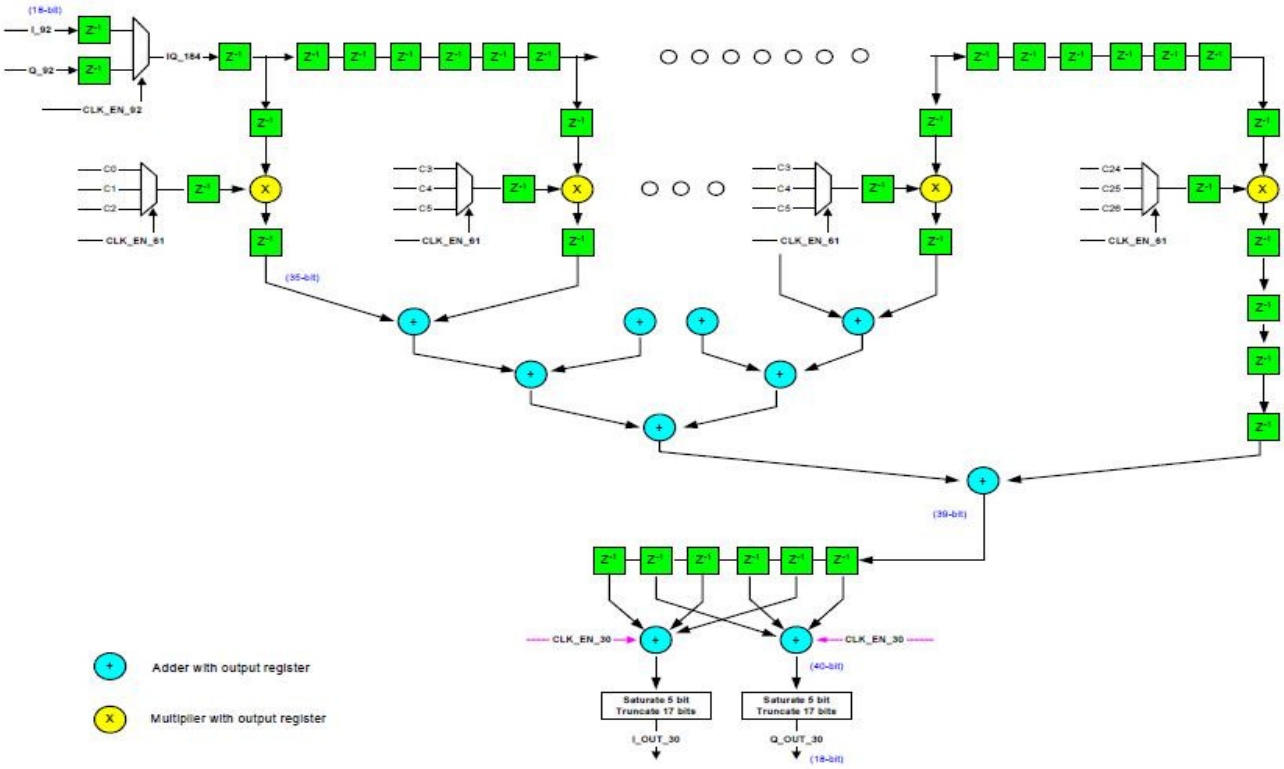

Figure 1. Architecture of a decimation-by-3 Polyphase filter

If a → 1, it is approximately a step response. If a → 0, the output changes gradually with input. Figure 2 depicts the details of an implementation of the first-order IIR filter. For general practice, the output of adder or multiplier needs to be registered before next processing element to meet the timing requirement. For the recursive structure in Figure 2, the feedback signal from the output has to get through at least one adder and one multiplier. This introduces two delay units as minimal. Double sampling rate technique is presented here to resolve this issue. The actual implemented function for the IIR is,

$$y_n = ax_{n-2} + (1-a)y_{n-2} \qquad (2)$$

It requires the filter operating at twice the original data rate. In fact, this double sampling rate IIR filter is effectively performing exactly the same as the original filter.

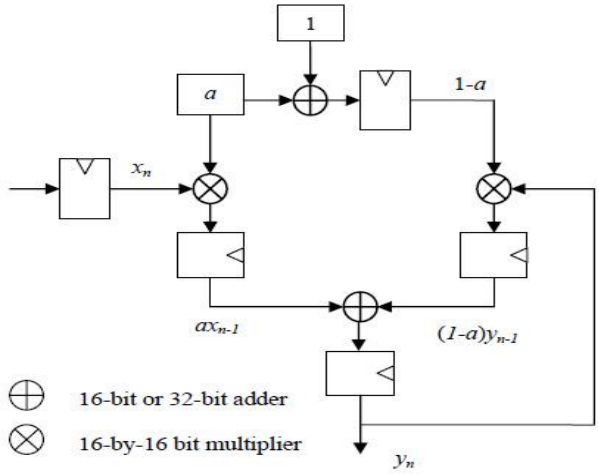

Figure 2. Architecture of a double sampling recursive IIR

Generally, pipelined structure can be applied to increase the throughput of the system in the price of more output delays. Parallel architecture is selected to reduce the number of circuit elements while increasing its operating speed. The recursive system presented above meet the performance requirement by increasing the sample rate. These are common trade-offs and solutions for VLSI implementation of signal processing algorithms.

VI CONCLUSION

Advances in application-specific integrated circuit (ASIC) are continually moving global communication technologies towards its ultimate goal: to securely transfer data, voice and image information to anywhere at anytime. This industrial evolution relies on VLSI signal processing research to provide efficient algorithm and to accommodate it into silicon dies. This paper provides a general review of recent advances in VLSI signal processing. It mainly includes high-speed low-power VLSI design for digital signal processing, DSP and communication block set IP core design, and telecommunication ASIC devices. For next generation mobile communication, analog components are pushed towards the front-end antenna. Digital transceiver is taking over the main signal processing tasks. Therefore, VLSI signal processing plays an important role in the mix of next generation wireless communications. Collaborations between algorithm and VLSI designer are aimed to reduce the overall product cycle of advanced signal processing technologies. As the device clock rate and gate capacity increases, it relies on the research in VLSI signal processing to fully realize its potentials.

In conclusion, VLSI signal processing is a promising technique including both signal processing algorithms and VLSI design methodologies. Current research in the area leverages contemporary semiconductor, VLSI, DSP and communication technologies in an effort to support the ever increasing demand of telecommunication systems. However, there still remain many challenging issues in system modeling, architectures, and emulation techniques. Research in this area is likely to continue making impact on the next generation wireless communication systems.

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