Design and Simulation a 1.9 GHz Class-E Power Amplifier

Seyed Reza Hadian Amrei, Masoud Sabaghi,Monireh Sadat Miri, Zahra Mobini Seraji and Mehdi Rahnama

Abstract—In this paper Class E amplifier was designed using Motorola's LDMOS (Laterally Diffused Metal Oxide Semiconductor) transistor models and its performance was simulated using ADS. A Class E power amplifier design that meets the CDMA specifications is described in this paper. Various procedures involved in the design of the Class E amplifier such as DC simulation, bias point selection, source-pull and load-pull characterization, input and output matching circuit design and the design of suitable harmonic traps are explained. The final amplifier implemented was a device operating at 1.9 GHz. In general the amplifier achieved its intended design specifications producing 220 mW with a power added efficiency of 58%.

Index Terms—ADS, Class E Power Amplifier, LD MOS, CDMA

1 INTRODUCTION

Class E power amplifiers are fundamentally dif ferent from the other types of power amplifiers discussed, it was seen that the operational differences were obtained by the selection of the bias point. However, in a Class E amplifier, only circuit-independent signal guidelines are given (discussed below), and the topology is not as restricted. The idea behind the Class E amplifier is to have non-overlapping output voltage and output current waveforms, and to limit the values of the voltage, current, and the derivative of the voltage with respect to time at the instants when the transition between non-zero currents and non-zero voltages occurs [1]. In [2], the first published work on Class E amplifiers; the important conditions for Class E operation are listed. These conditions are based on the assumption that the transistor acts like a switch for Class E operation. Also the terms "on" state and "off" state are used to describe the time period when the transistor starts conducting and stops conducting respectively. The voltage across the switch must return to zero just before the switch turns "on" and starts conducting current. Similarly the current through the switch must return to zero just before the switch turns "off". These two conditions avoid the energy dissipation caused by the simultaneous superposition of substantial voltage and current on the switching transistor during transition from "on" to "off" state or "off" to "on" state. Another condition for Class E operation is that the voltage across the switch must return to zero with zero slope (i.e., dv/dt = 0). Hence the current through the transistor at the beginning of "on" state is zero. Similarly the current through the transistor must return to zero with zero slope (i.e., di/dt = 0) and the voltage across the transistor at the beginning of "off" state is zero. Hence for a deviation in the switching instant from the ideal switching time the corresponding output voltage or current will be very small, and the power lost in the device due to this non-ideality will be relatively small [2]. With all these conditions satisfied, very high efficiencies can be achieved. However it is quite difficult to meet all these requirements in practice. The maximum theoretical efficiency of Class E amplifiers is 100% [3], however efficiency values around 60% are typically achieved.

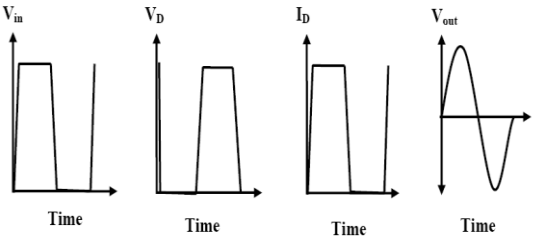

Fig. 1. Frequency Typical Class E Waveforms

In this Paper, a highly efficient class E power amplifier has been designed for CDMA band with a center frequency of 1.9 GHz and bandwidth of 5 MHz using LDMOS transistor. The amplifier has been simulated using a high frequency circuit simulator namely, the Agilent Advanced Design System (ADS2009).

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2 CLASS-E OPERATION

Fig. 1 shows a conceptual picture of a class-E power amplifier [2], [4]. In operation, the input signal toggles the switch periodically with approximately 50% duty cycle. When the switch is on, a linearly increasing current is built up through the inductor. At the moment the switch is turned off, this current is steered into the capacitor, causing the voltage across the switch to rise. The tuned network is designed such that in steady state, returns to zero with a zero slope, immediately before the switch is turned on. The bandpass filter then selectively passes the fundamental component of to the load, creating a sinusoidal output that is synchronized in phase and frequency with the input. In practical applications, may be phase or frequency modulated, in which case the information embedded in the modulation is also passed to the output with power amplification.

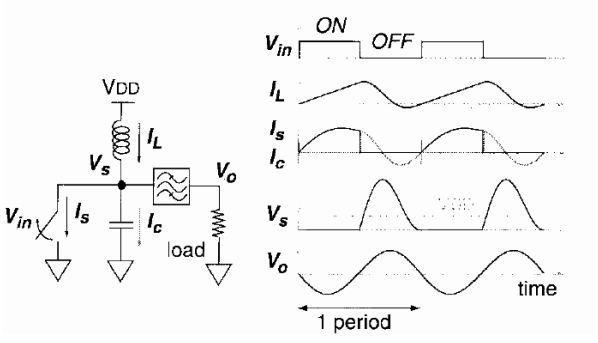

Fig. 2. A simplified class-E PA and its steady-state operation.

3 CLASS-E PA CHARACTERISTICS

By comparing and in Fig. 2, one observes that in principle, the switch voltage and the switch current are never simultaneously nonzero. Since the instantaneous power dissipation of the switch is the product of these two quantities, the switch is ideally lossless, and all the power from the dc supply is delivered to the radio-frequency (RF) output. In addition, the capacitor is designed to be fully discharged before the switch is turned on. This property, commonly known as "soft switching," eliminates any discharging energy loss.

In high-speed operation, the switch transition time can become a significant fraction of a signal period. During these transitions, the switch voltage and current may be simultaneously nonzero, causing potential power loss in typical switching amplifiers. Class-E PA's however are designed to minimize this loss. At the turn-on transitions, loss is alleviated by a zero switch current resulting from the simultaneously zero and On the other hand, turnoff transition loss is reduced by delaying the switch voltage rise until the switch is turned off. These properties have made class-E PA's attractive for high-speed, high-efficiency operations [5], [6].

In the case that the switch is implemented in CMOS, the soft switching action of a class-E PA ensures that the MOS transistor is in the triode region when the switch is turned on, acting as a simple resistor. This is in contrast to hard-switched switching amplifiers (e.g., class D), where the transistor momentarily resides in the saturation region acting as a current source during the turn-on transitions. This property enables a class-E PA to be modeled and analyzed as a circuit whose topology toggles between the two linear LRC networks, as shown in Fig. 3 [7]–[9].

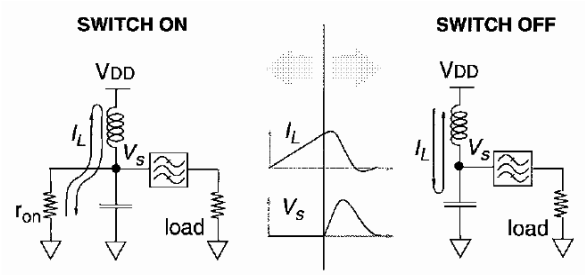

Fig. 3. A class-E PA modeled as toggling between two linear LRC networks

4 CLASS-E IMPLEMENTATION

The various design blocks of the Class E amplifier were explained. The final design was realized in ADS. The PA uses Motorola's High Voltage Version10p04 LDMOS transistor model. Non-ideal inductors with a Q of 20 were used so that the results obtained are close to the performance obtained using commercial inductors. The Class E amplifiers use identical transistors, bias points and input and output matching networks. Figure 4 show the final realization of the Class E designs respectively. These designs will be simulated and the results will be analyzed.

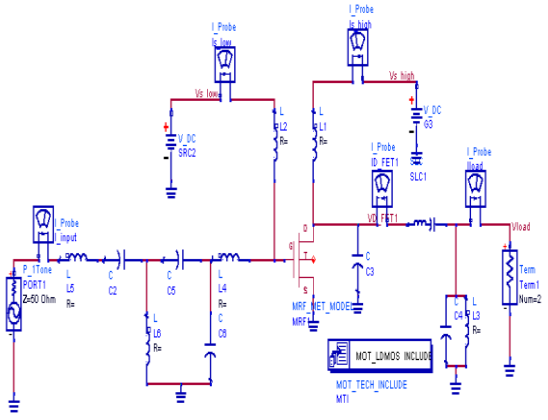

Fig. 4. Schematic of the Class E power amplifier Design

4.1 S-parameter simulation

Figure 5 shows simulated S-parameters Class E power amplifier. As can be seen in Figure. 5, S21 is above 18dB at 1.9GHz, input and output impedance matching (S11,S22) is below -8dB at 1.9GHz. Figure 6. Shows Noise Figure and reveal that NF is close to 2.6dB from 1-3GHz .NFmin is below 1.835dB at 1.9GHz.

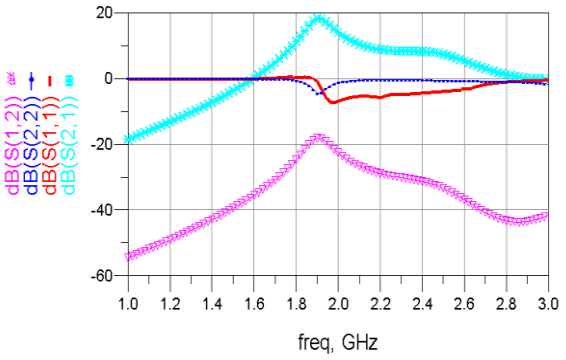

Fig. 5. S-parameter of Class E power amplifier

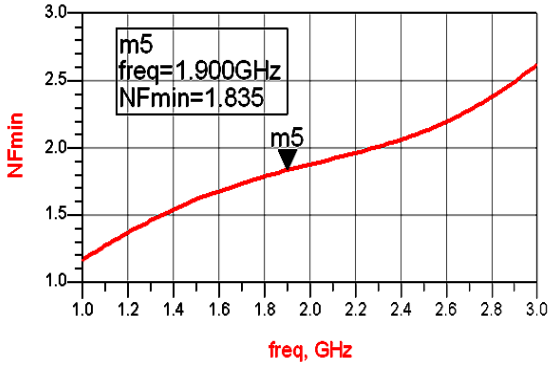

Fig. 6. Noise Figure of Class E power amplifier

4.2 Harmonic Terminations

In class E amplifier the second and third order harmonics tuning need to be included in the output network to increase output power and efficiency.

The design of proper harmonic traps is the most crucial and also the most difficult aspect of the design. The third harmonic trap was designed using a parallel L-C filter tuned at the third harmonic frequency of 5.7GHz. Several combinations of L and C that would resonate at this frequency were designed. Of these, the combination which gives the best performance using as small an inductor as possible was chosen. For the second harmonic trap, a series L-C filter tuned at the second harmonic frequency of 3.8GHz was initially designed. However, it was noted that there was considerable fourth harmonic current in the circuit, causing power loss. In order to overcome this, a transmission line one quarter-wavelength long at fundamental frequency was tied to the drain of the transistor with its other end bypassed to ground. This was able to provide a very good short circuit at not only the second harmonic frequency but also at the fourth and higher even order frequencies. A similar approach using a quarter-wavelength transmission line to provide an open circuit for odd harmonic frequencies was tried but it was observed that the transmission line was unable to produce a good open circuit.. Hence the third harmonic trap was realized using discrete components. Harmonic traps for the fifth and other higher odd harmonics can be included to improve the performance at the cost of increased circuit complexity. In [12], the trade-off between the number of odd harmonic traps and circuit complexity has been analyzed and it is found that the third harmonic trap is usually enough for acceptable Class F performance. In addition to increasing the circuit complexity, additional harmonic traps may result in loss when realized using practical components. Also at high operational frequencies, it may be impossible to realize the design using practical components. Considering these limitations the selected design scheme for the harmonic traps seems to be the best solution.

Figure 7 give the PAE plots of the Class E amplifiers respectively. There are Maximum PAE at 32 RFpower Where PAE=58%.

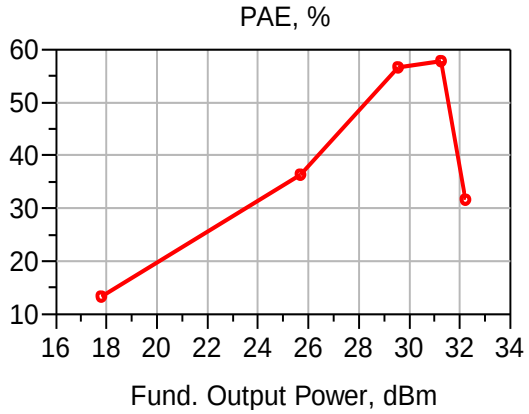

Fig. 6. Noise PAE (%) vs RF power (dBm)

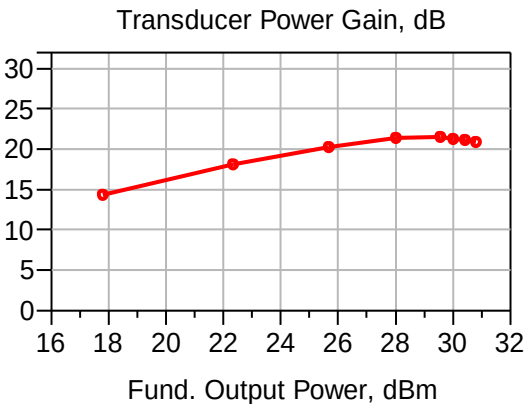

Fig. 7. Transducer power gain (dB) vs RFpower (dBm)

Figure 9 is a plot of the power supplied to the load, in dBm, at each frequency of the Class E Power Amplifier.

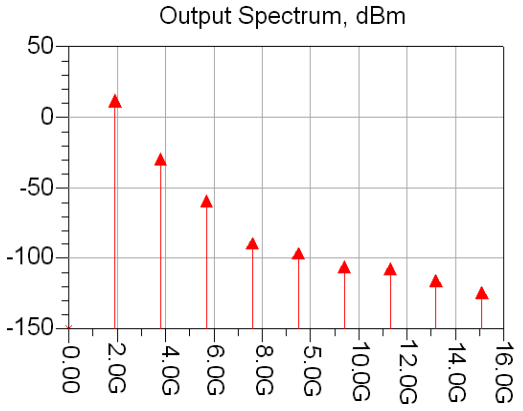

Fig. 8. Output spectrum

Table1 shows summarizes performance of Class E Power amplifier

TABLE 1. SUMMARIZES THE PERFORMANCE OF THE CLASS E

Performance Parameter	Performance
Output Power P_{out}(dBm)	37.6
Gain (dB)	20
Power Added Efficiency @ maximum output power (%)	58
DC Power P_{dc} (Watts)	3.17
Thermal Dissipation (Watts)	1.48
Input Power Pin (dBm)	18.8

TABLE 2.COMPARISON TO PREVIOUS WORK

	[11]	[10]	This work
Technology	0.18 um CMOS	0.35 um CMOS	LDMOS
Frequency(GHz)	1.9	1.9	1.9
Supply voltage	2.4	1	3
Efficiently	57%	40%	58%
Power gain (dB)	16	-	20
Output power (mW)	200	200	220
Architecture	Single ended	Single ended	Single ended

5 CONCLUSION

We designed and simulated a class-E amplifier. The amplifier has been simulated using a high frequency circuit simulator namely, the Agilent Advanced Design System (ADS). The research has proven by means of simulation, the feasibility of using a Class E amplifier for CDMA applications by achieving an efficiency of 58% with good linearity. This paper work provided the opportunity the make some important contributions in this field of research. The idea of using Class E amplifiers to improve efficiency without degrading linearity is relatively new and prior to this there has been no significant published work which focuses on Class E amplifiers for CDMA applications. Actual performance of the designed amplifier may vary significantly.

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